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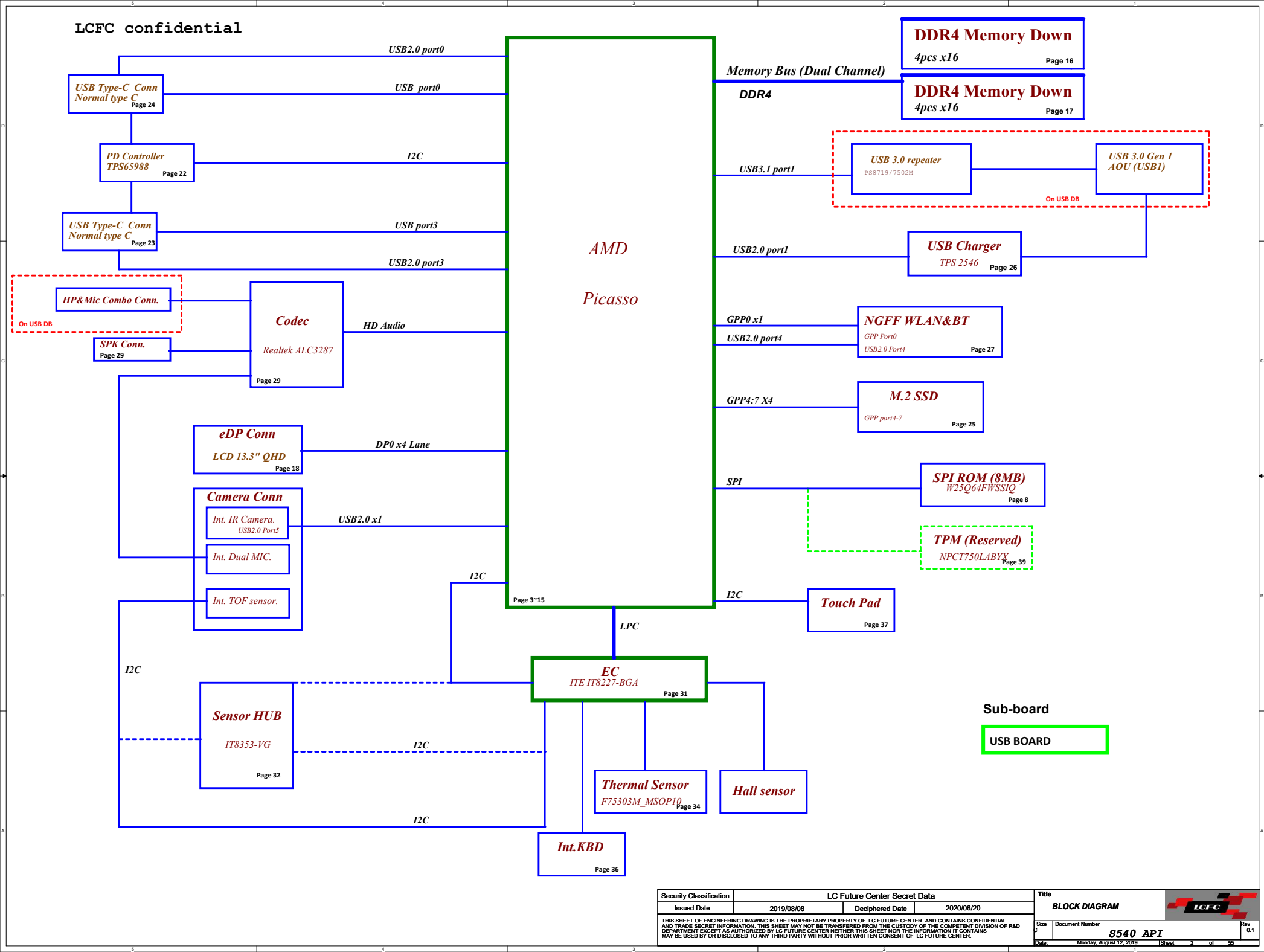
S540 13API/GS341 M/B Schematics Document

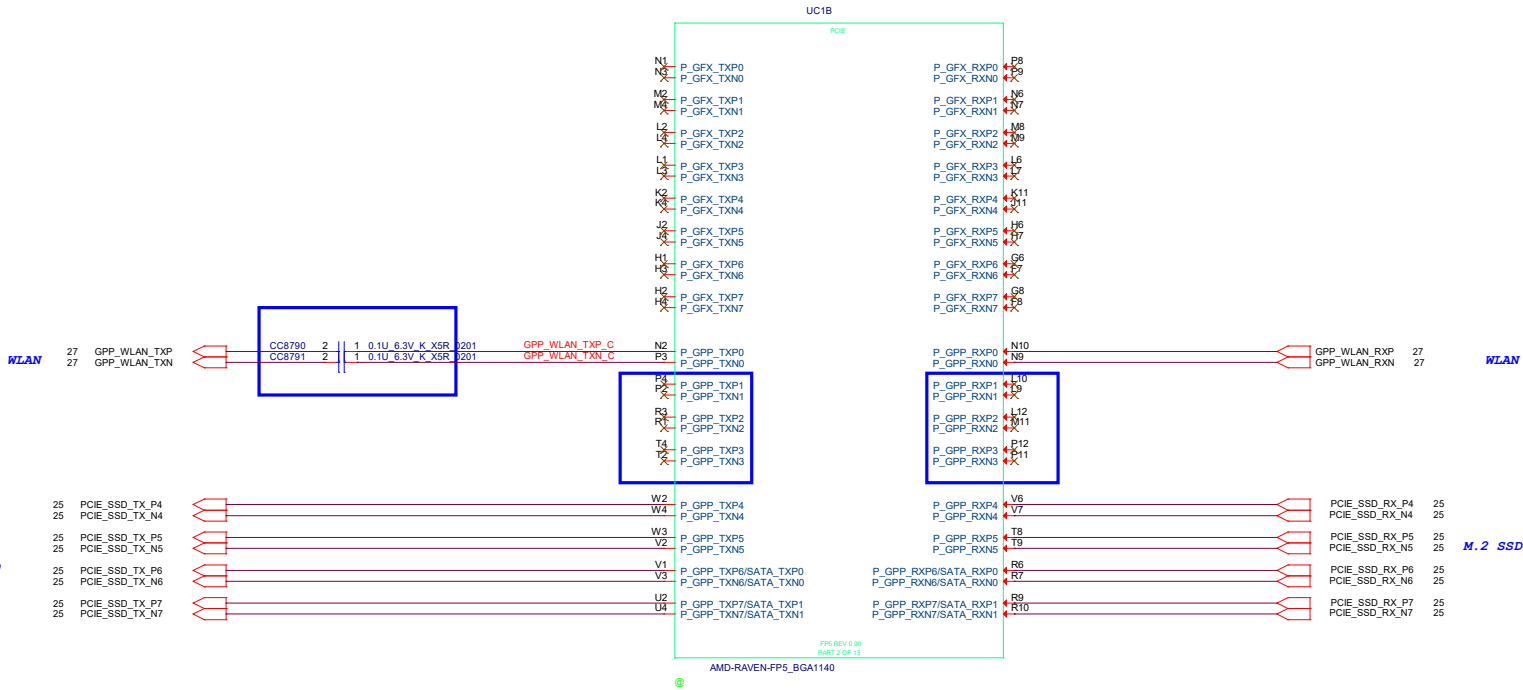
AMD FP5 PICASSO SOC with DDR4+UMA

2019-08-08

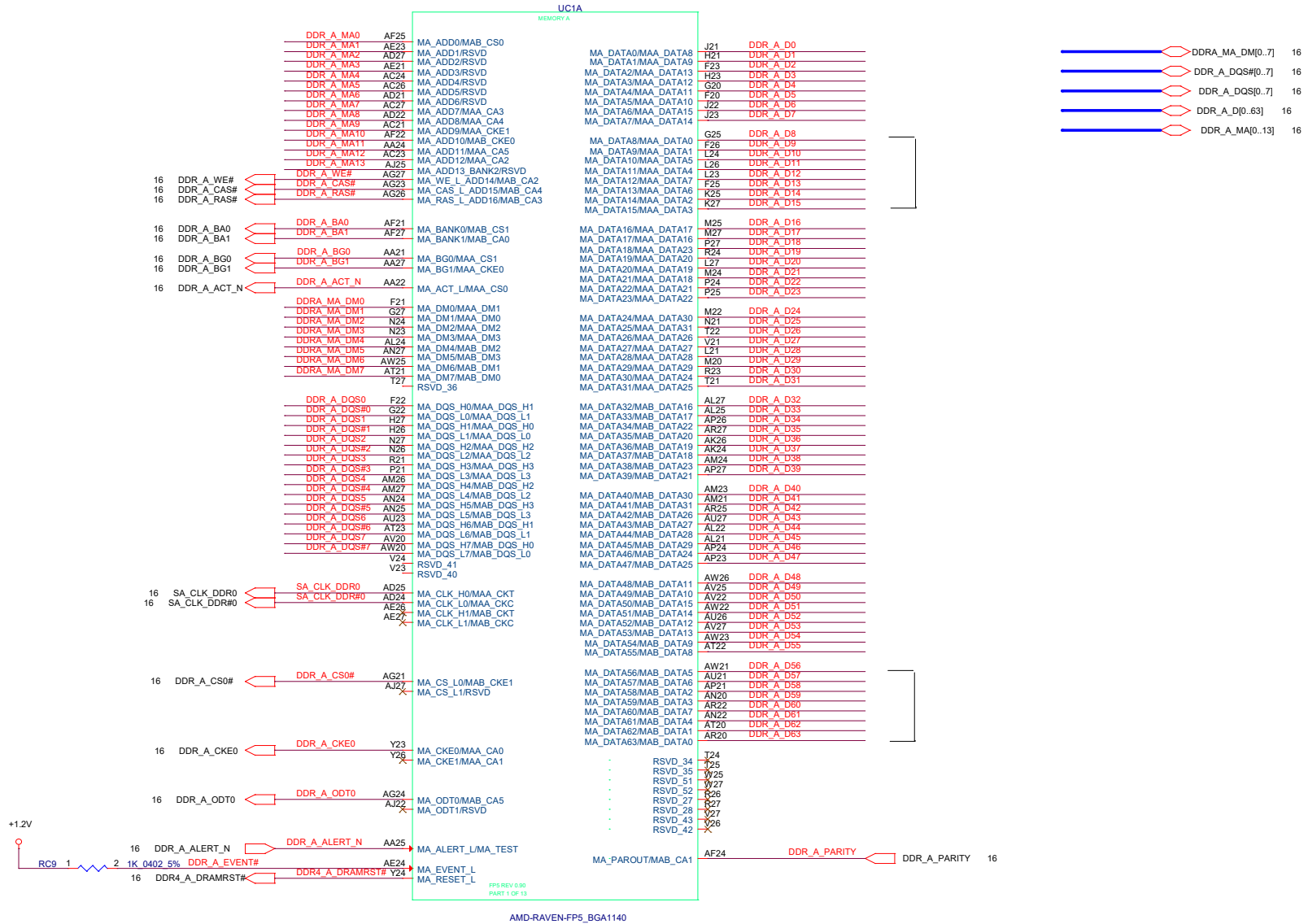
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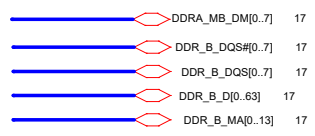
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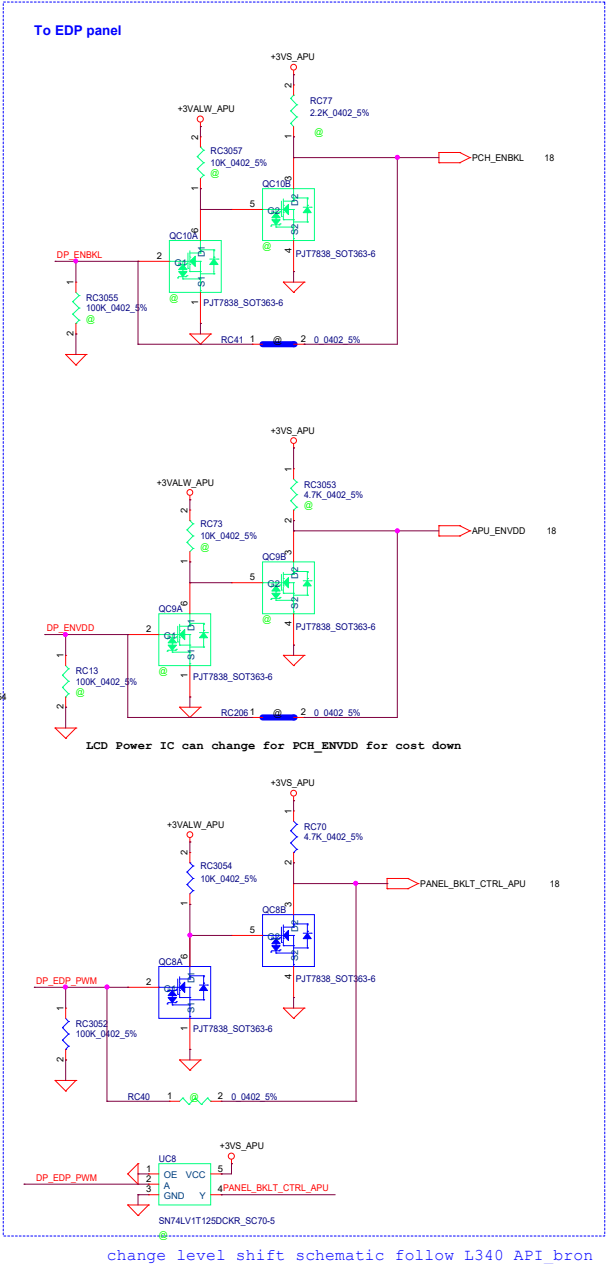
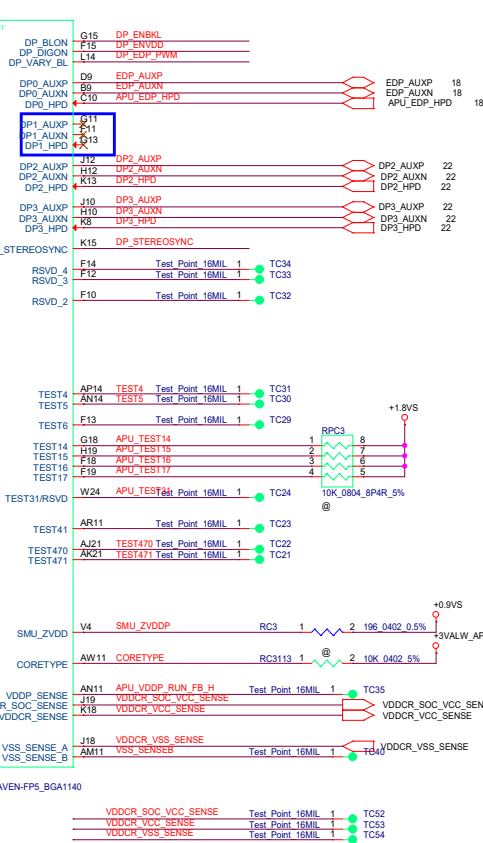





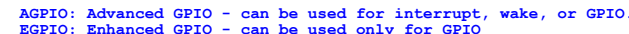
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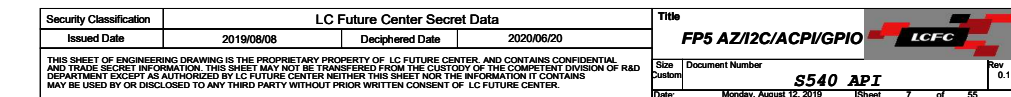


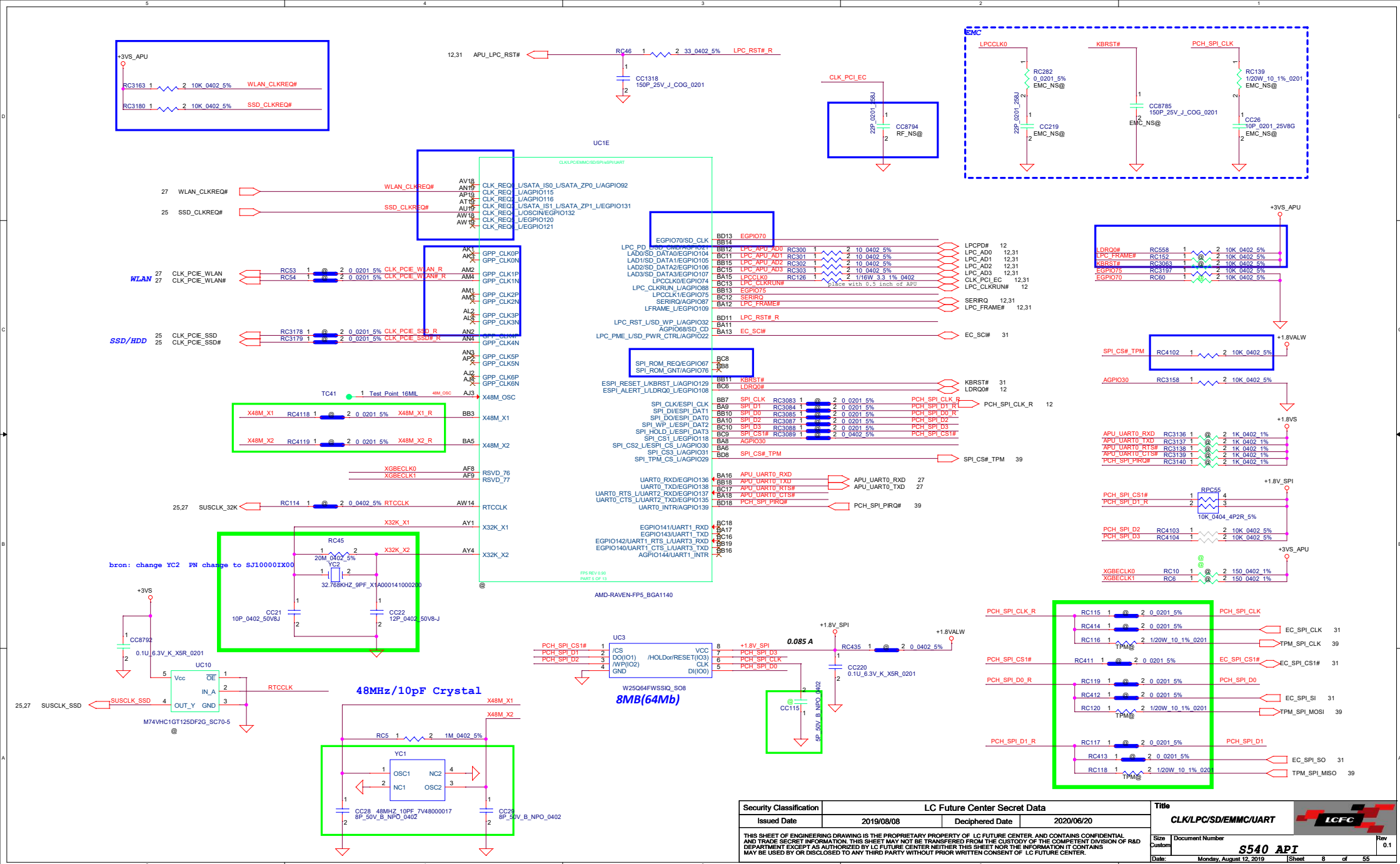



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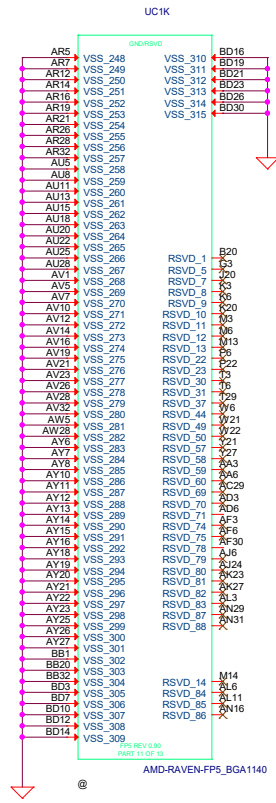
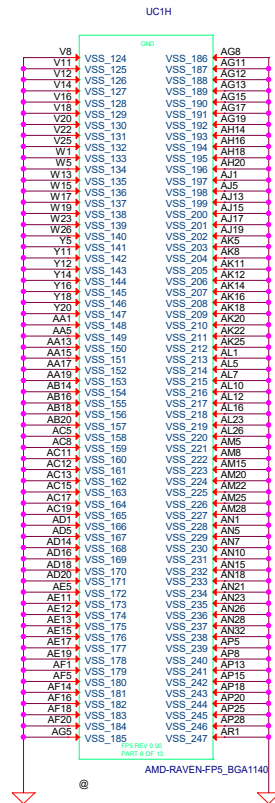
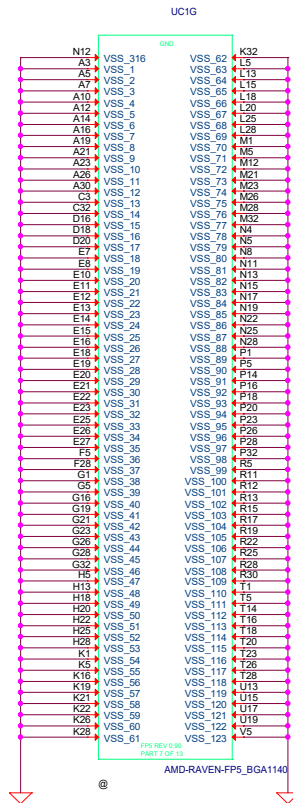


The schematic diagram illustrates the I2C bus configuration for the ADXL345 module. The bus consists of two lines: SDA (Serial Data) and SCL (Serial Clock). The SDA line is connected to the module pins RC1616, RC1614, RC1612, RC1610, RC1608, RC1606, RC1604, and RC1602. The SCL line is connected to the module pins RC1615, RC1613, RC1611, RC1609, RC1607, RC1605, RC1603, and RC1601. Both lines are terminated with 10K 0402 5% resistors at both ends. The module is powered by +3V3L_W APU and +3V3L APU. The module pins are labeled BOARD_ID0, BOARD_ID1, BOARD_ID2, BOARD_ID3, BOARD_ID4, and BOARD_ID5.

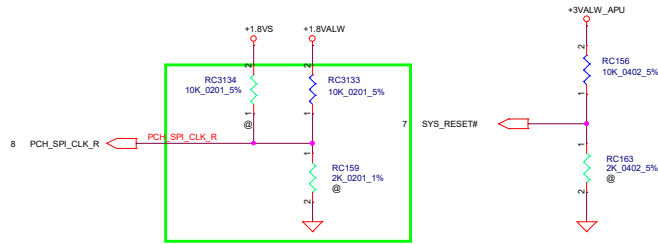




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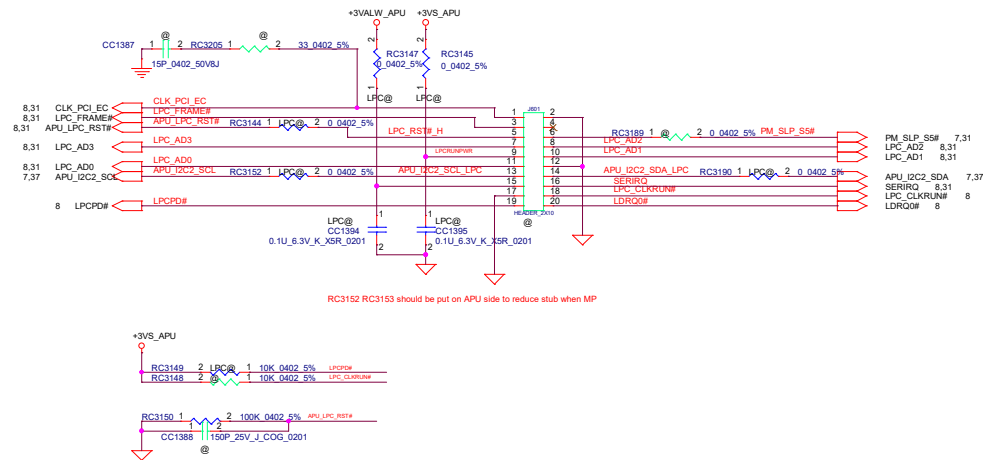


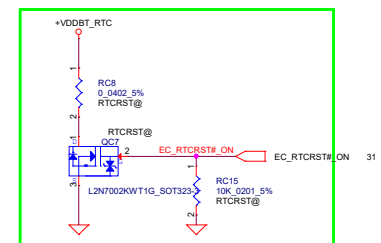
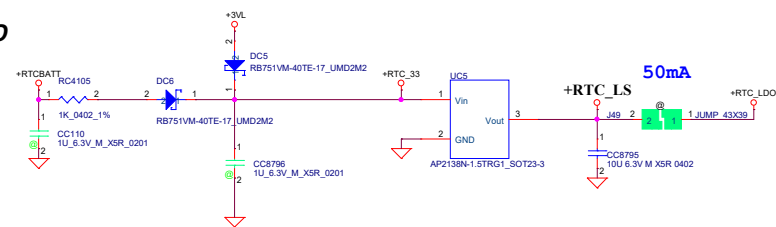
STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE (DEFAULT) 0:SHORT RESET MODE


LPC ROM EMULATOR HEADER

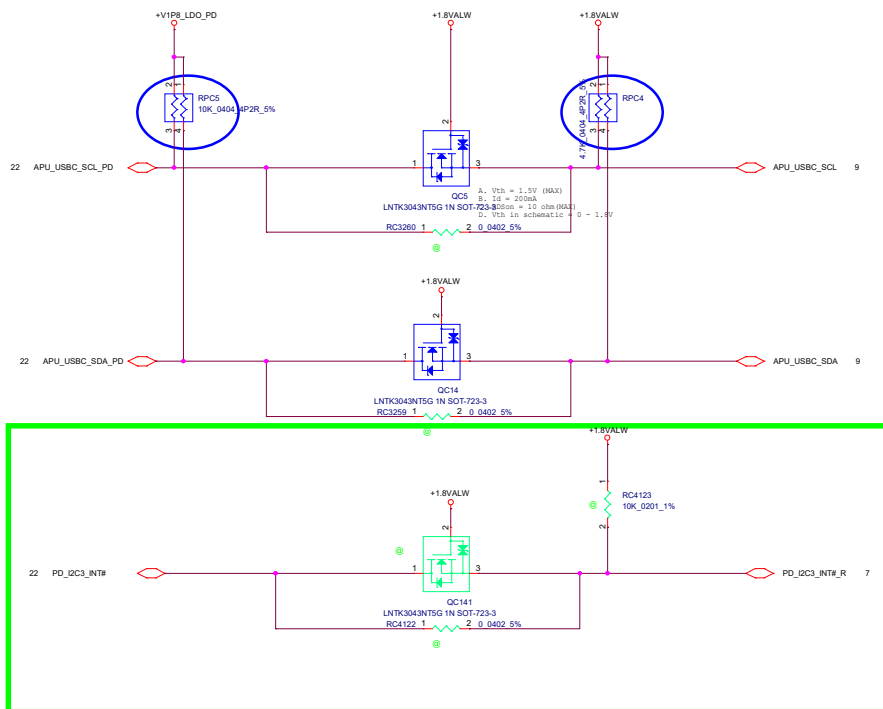
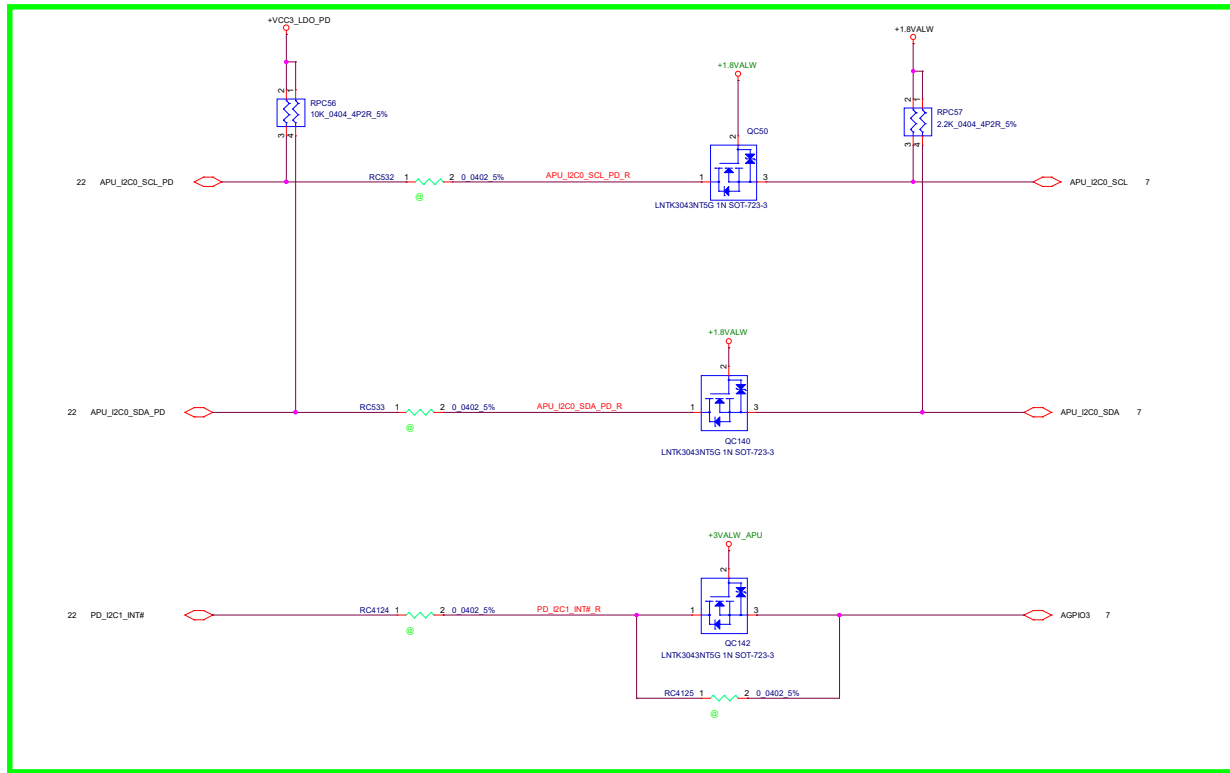
PIN4 should be removed as a Key

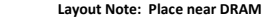
DAISY CHAIN ROUTING FOR LPC SIGNALS






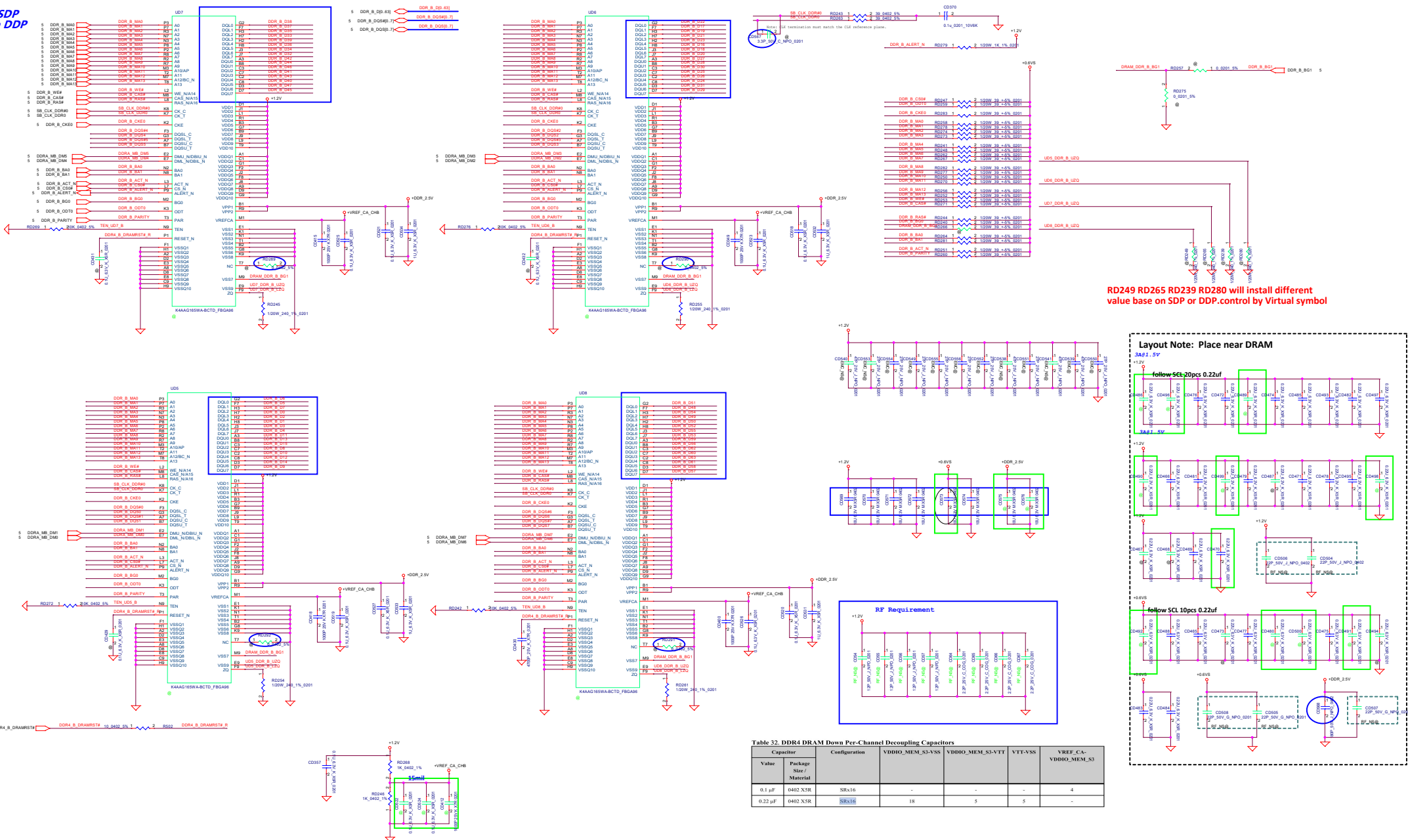
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Capacitor		Configuration	VDDIO_MEM_S3-VSS	VDDIO_MEM_S3-VTT	VTT-VSS	VREF_CA-VDDIO_MEM_S3
Value	Package Size / Material					
0.1 μ F	0402 XSR	SRx16	-	-	-	4
0.22 μ F	0402 XSR	SRx16	18	5	5	-

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<div style="text-align: right;">Date: Monday Aug 12, 2019 Sheet: 18 of 35</div>					Rev: 0.1



RD249 RD265 RD239 RD280 will install different value base on SDP or DDP, control by Virtual symbol

Layout Note: Place near DRAM

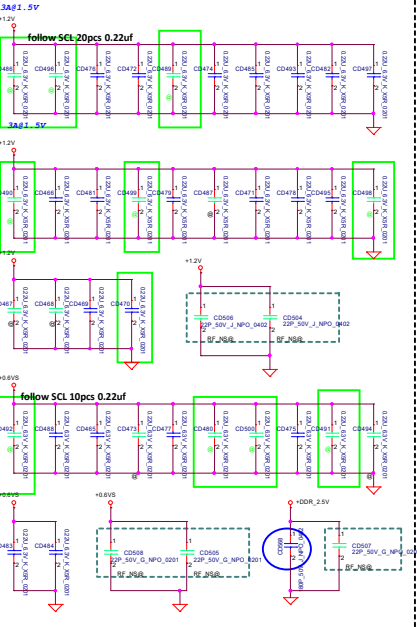
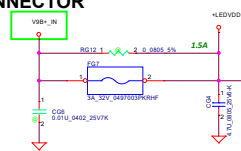


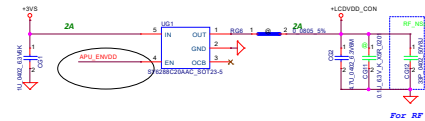
Table 32. DDR4 DRAM Down Per-Channel Decoupling Capacitors

Capacitor	Configuration	VDDIO_MEM_S3-VSS	VDDIO_MEM_S3-VTT	VTT-VSS	VREF_CA-VDDIO_MEM_S3
Value	Package Size / Material				
0.1 μ F	0402 XSR	SRa16	-	-	4
0.22 μ F	0402 XSR	SRa16	18	5	5

LCD CONNECTOR

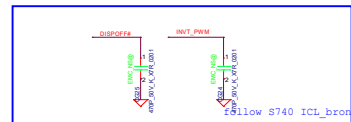
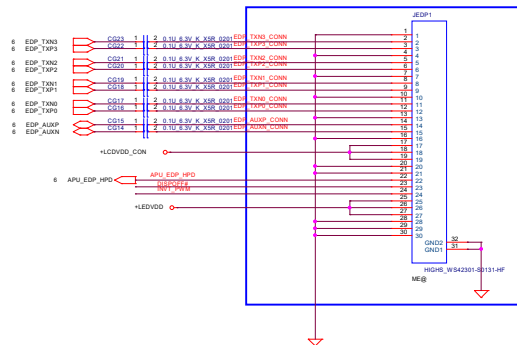


LCDVDD Circuit

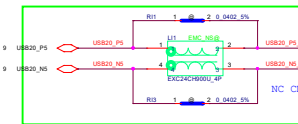
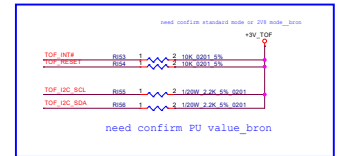
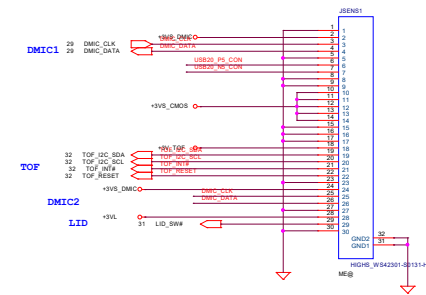
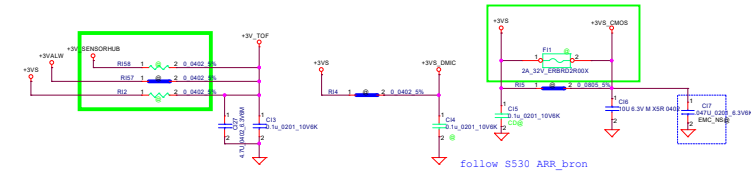


follow L340 API_bron

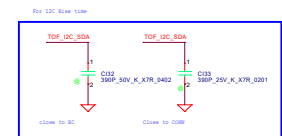
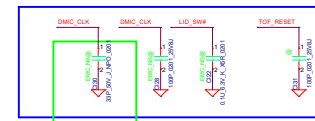
APU output enable Voh min is 1.8V-0.45V=1.35V





CAMERA CONNECTOR

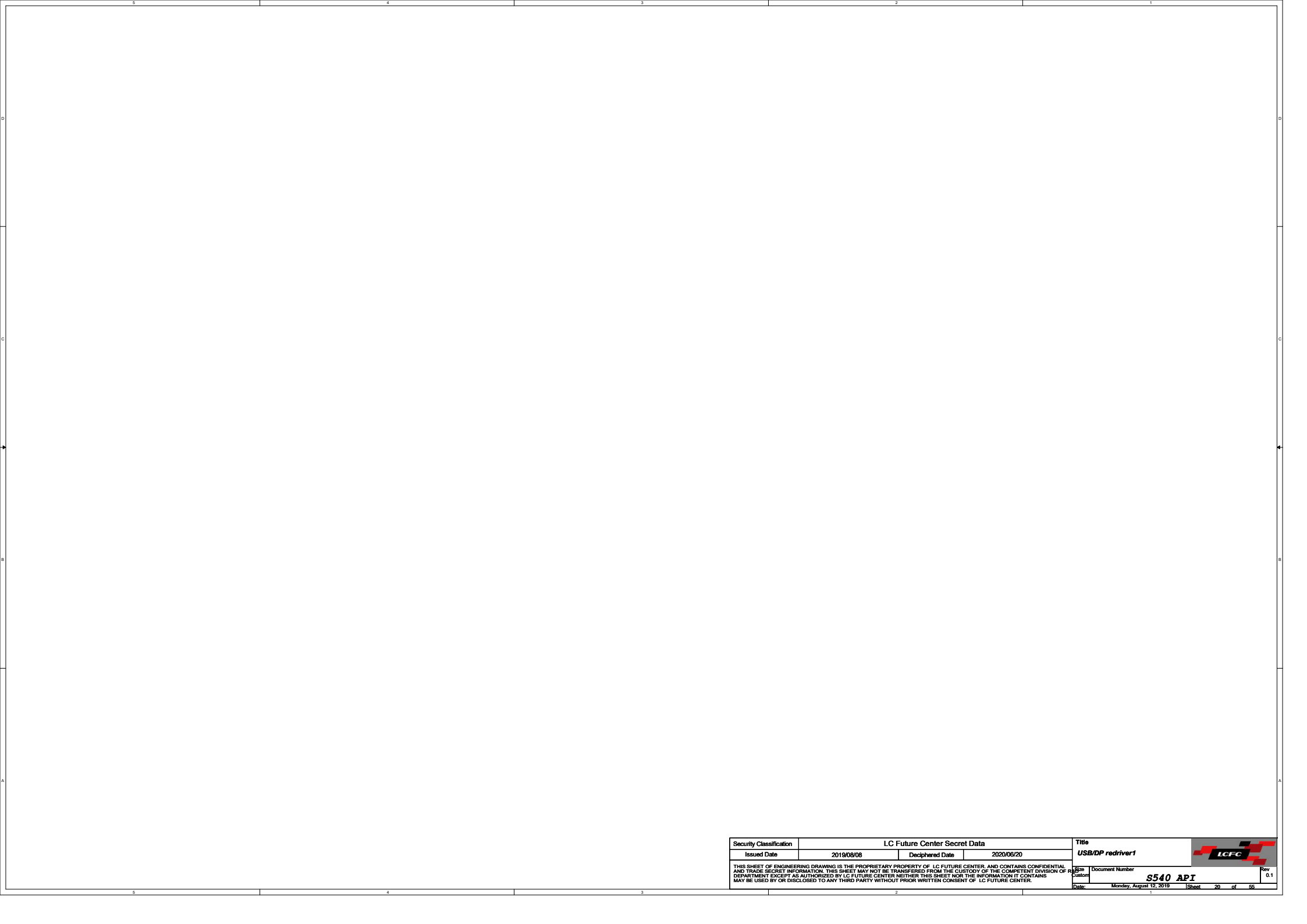



EMI request




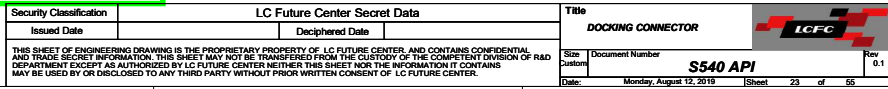
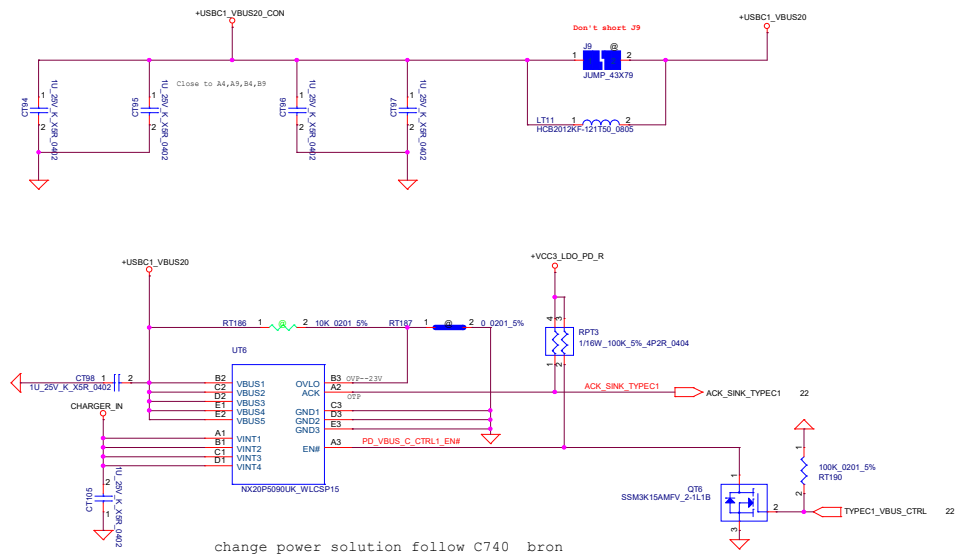
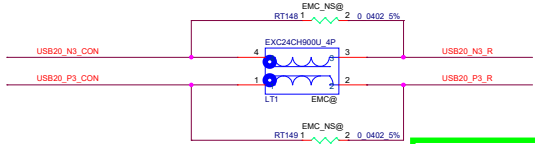
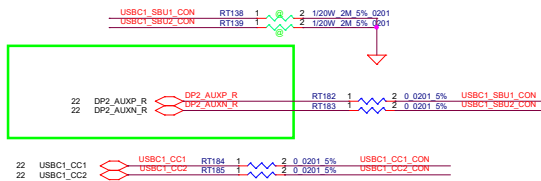
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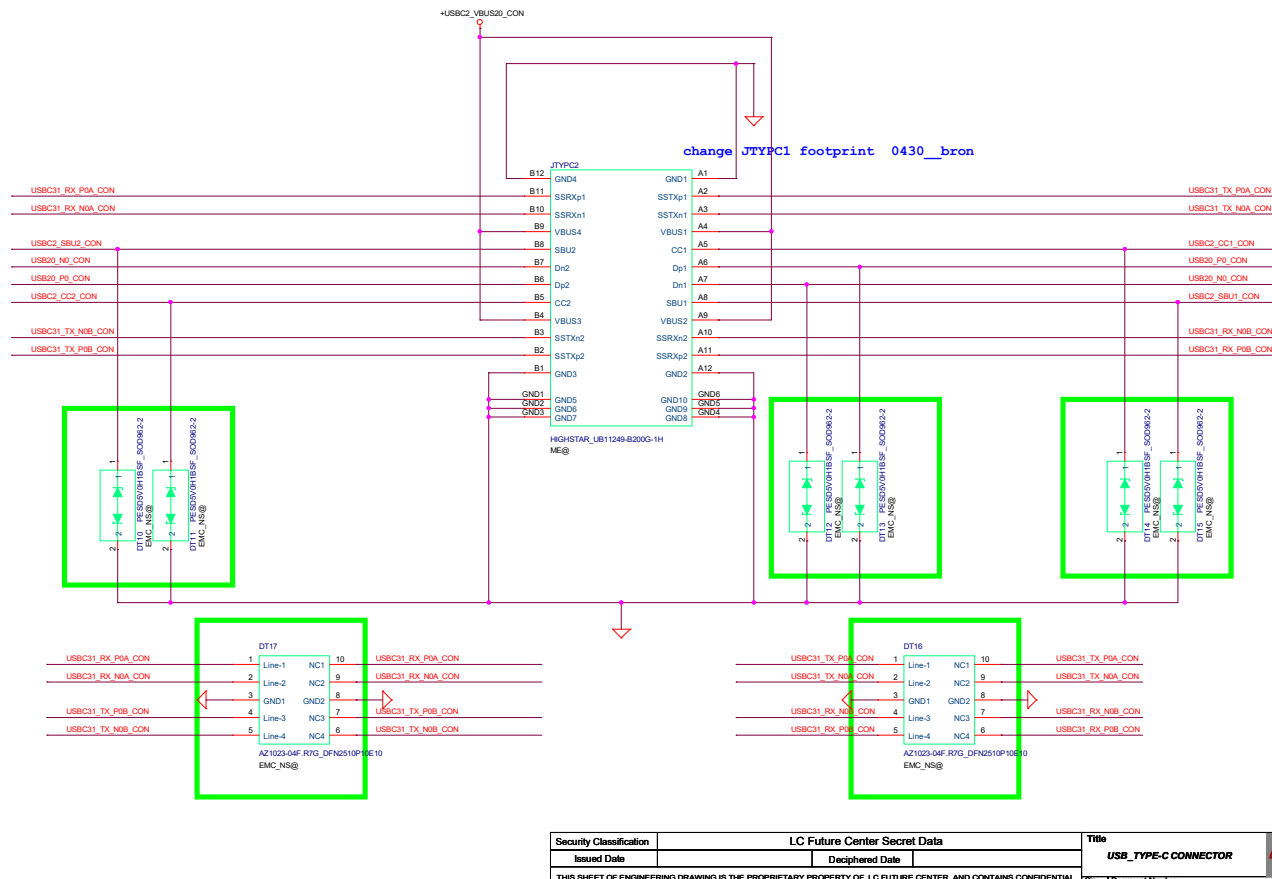
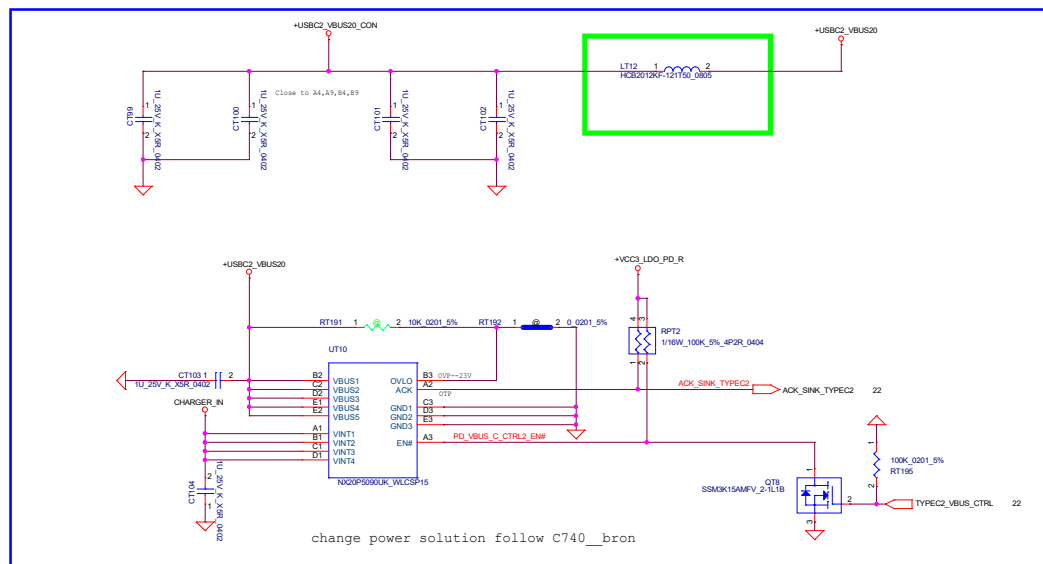
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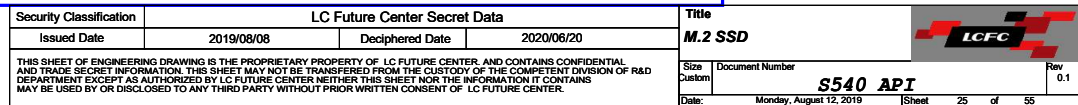
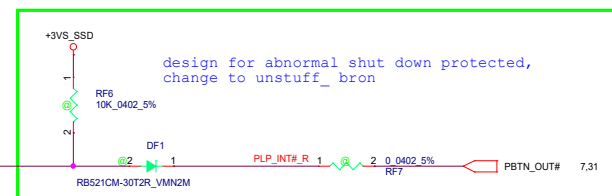
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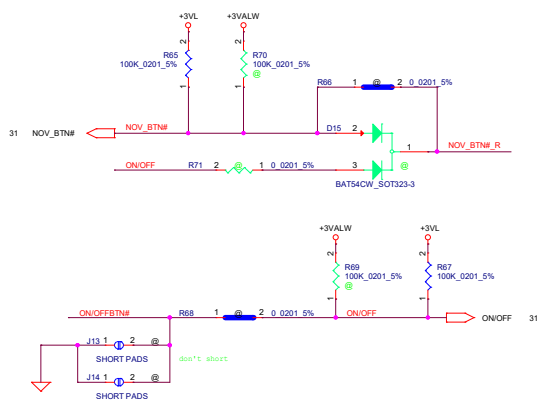
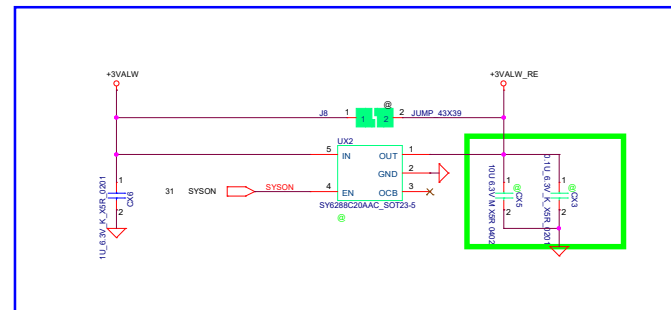
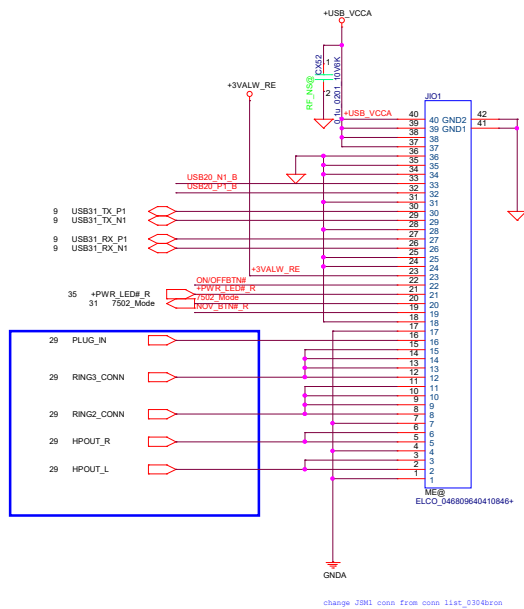
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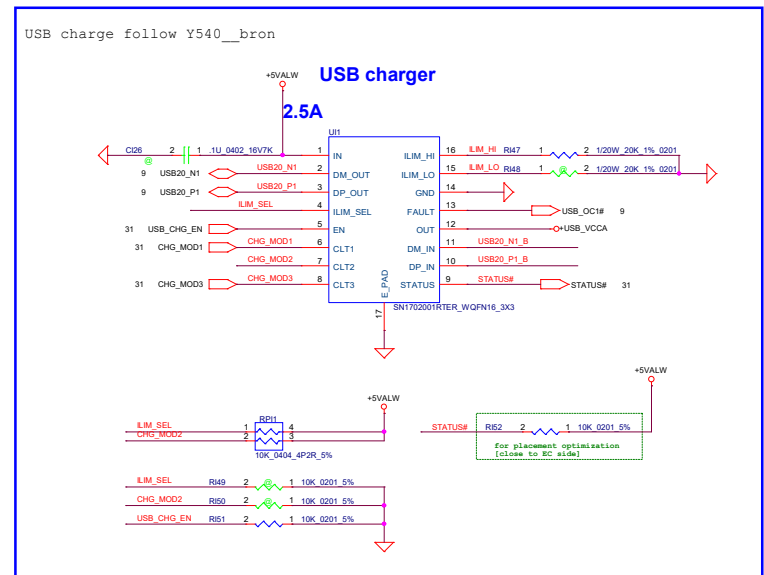



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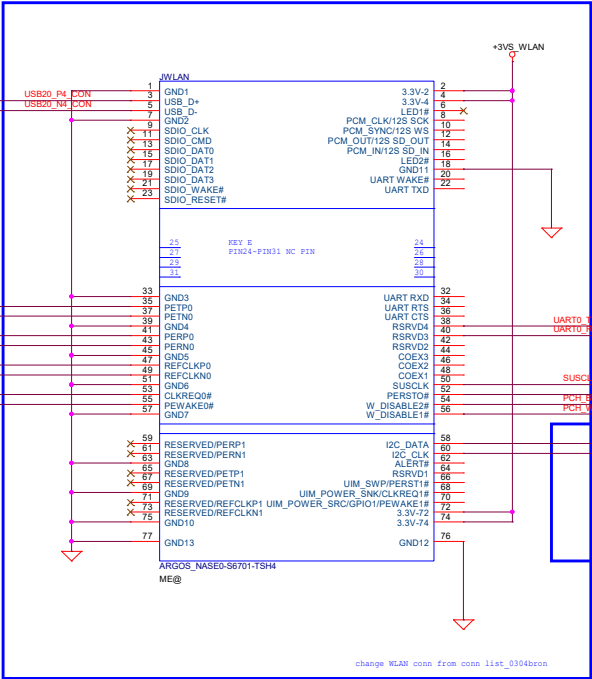
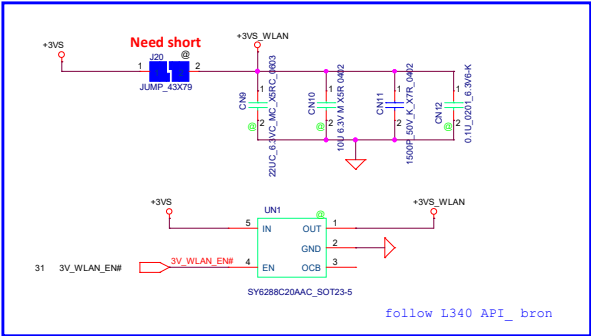


CLT1	CLT2	CLT3	ILM_SEL	MOD	
0	0	0	X	DCN	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

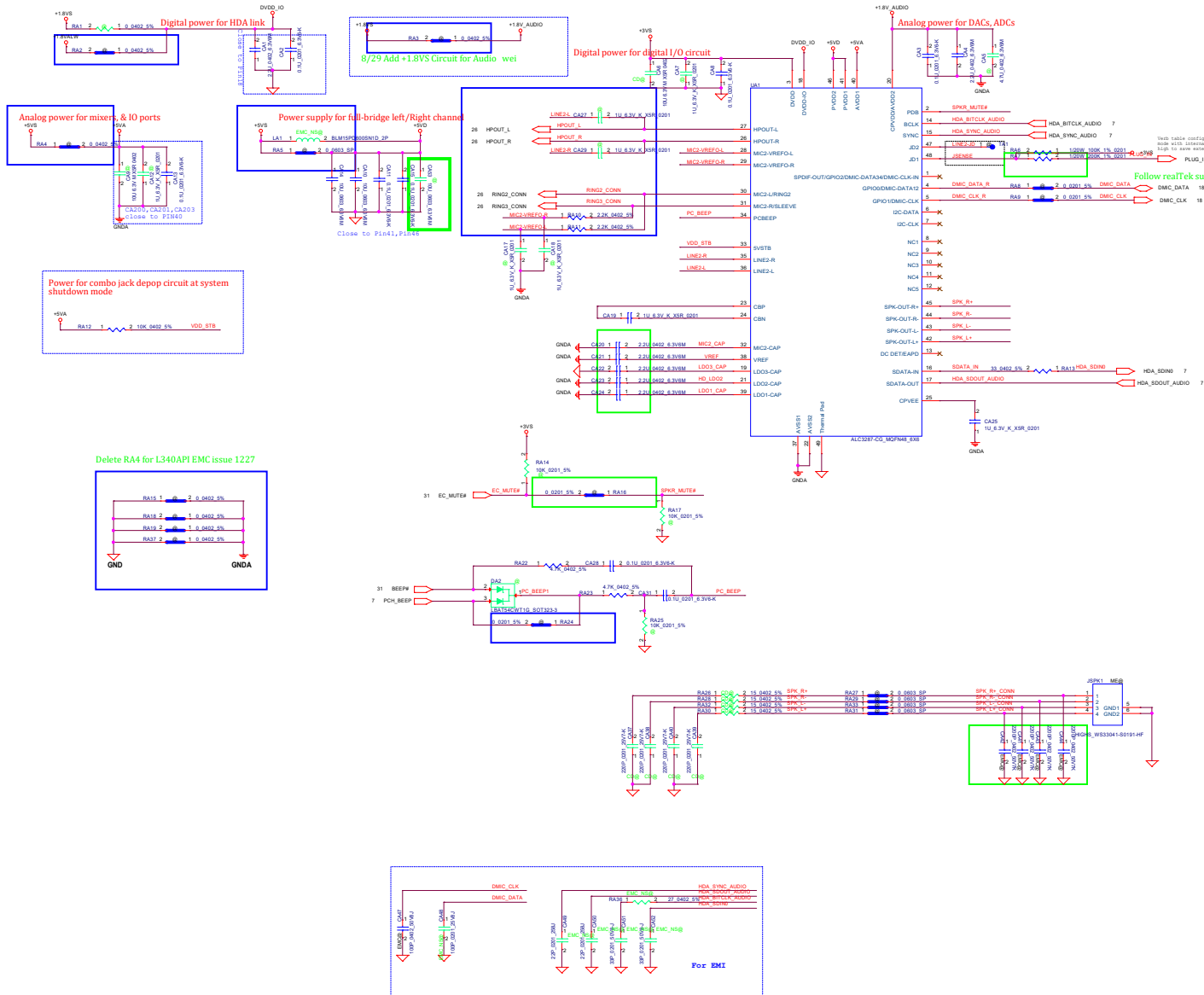


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				Rev 6.1 Mends: August 31, 2019	

Mini-Express Card(WLAN/WiMAX)



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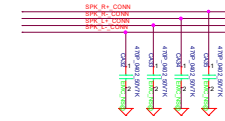


Verb table configures as 1.05
mode with internal 1.0V pull
high to save material costs.

Follow realtek suggest, change CA205 to 0.22u

20pin Audio Jack: Verb table configures as 2 JD
R0000

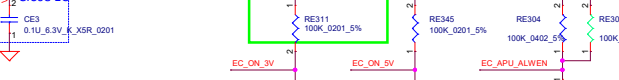
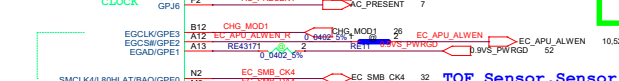
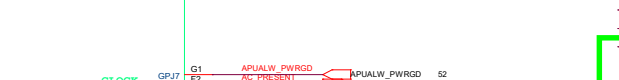
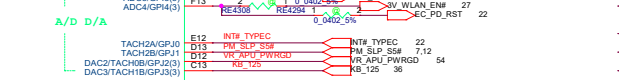
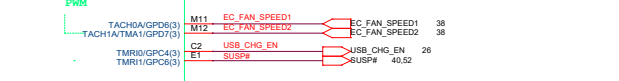
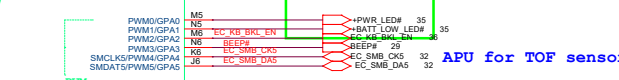
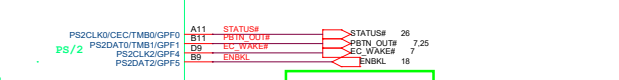
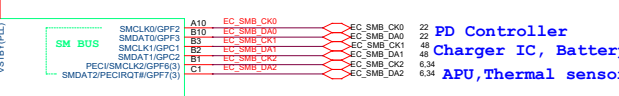
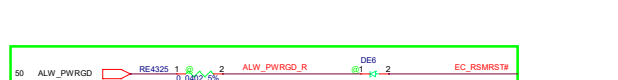
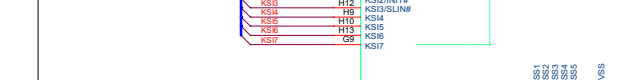
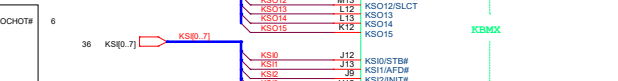
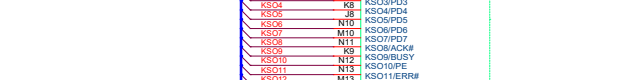
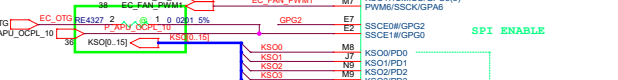
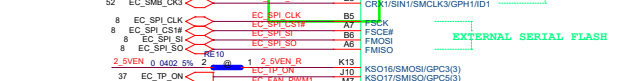
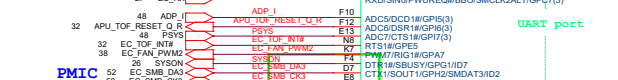
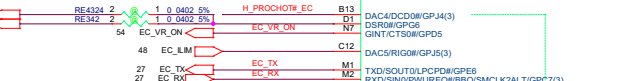
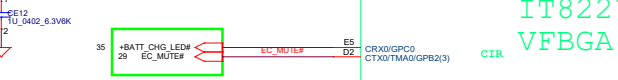
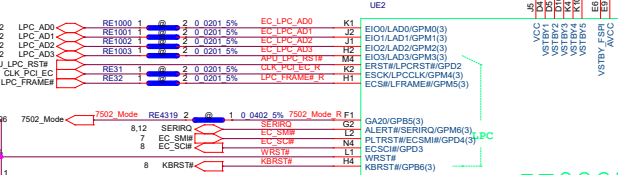
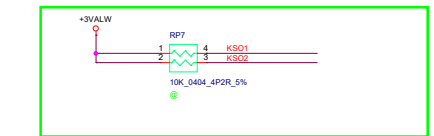
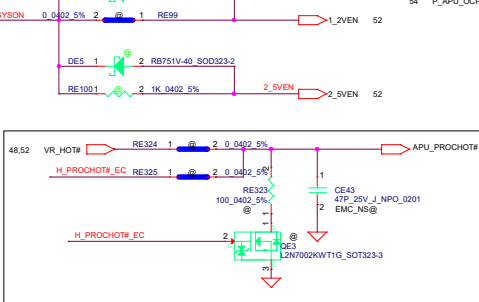
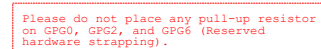
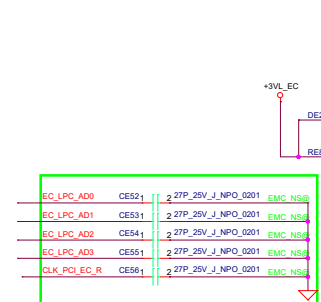
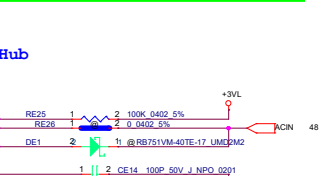
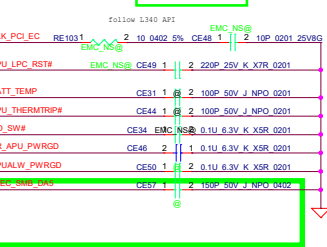
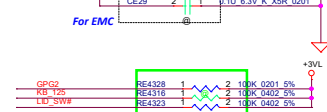
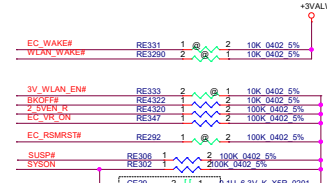
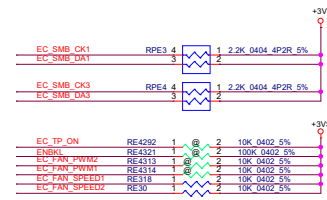
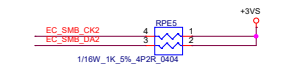
Reserve for L340API SPKR EMC noise 0912




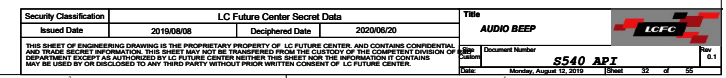


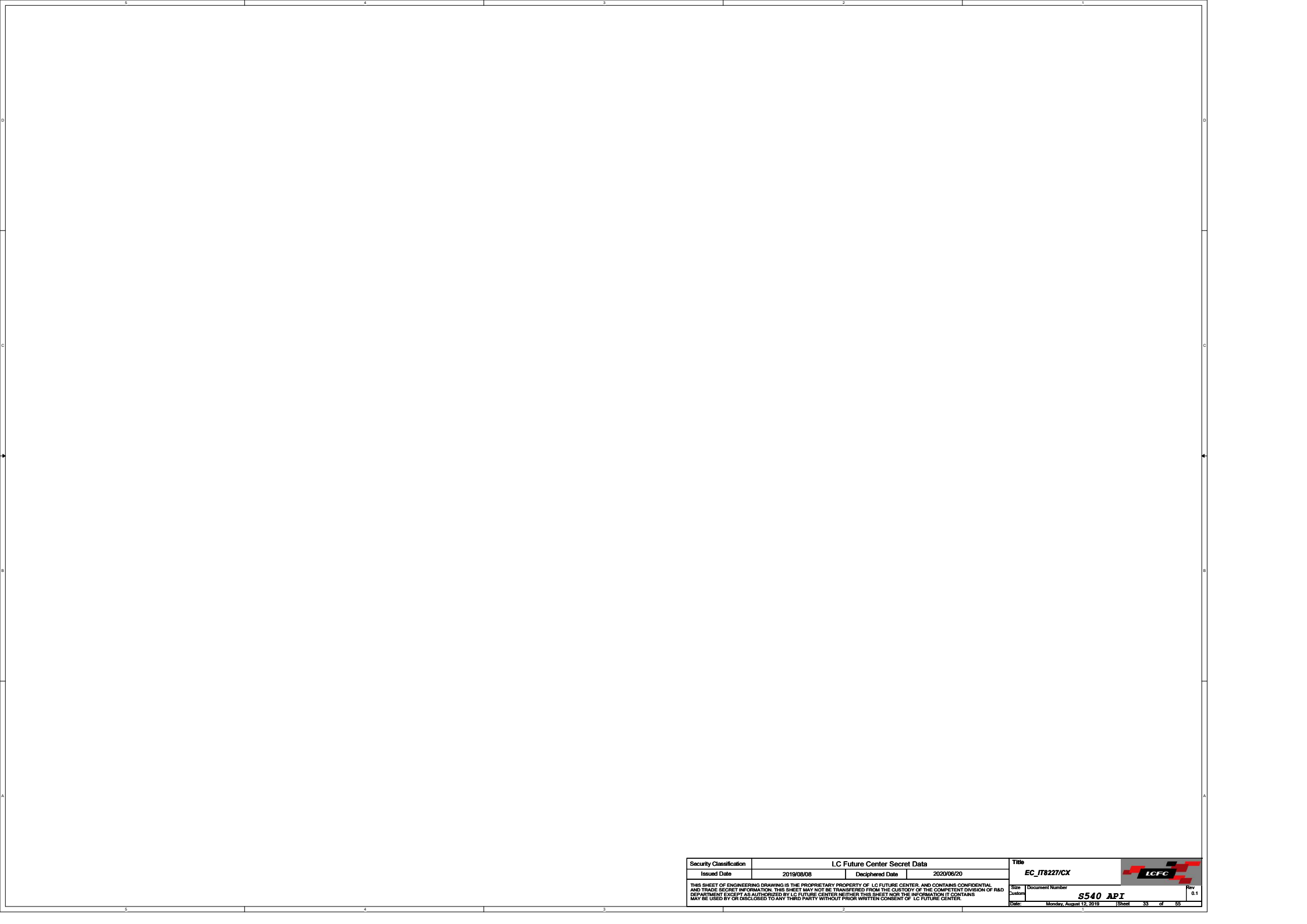
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Issued Date	2019/08/08	Deciphered Date	2020/06/20	AUDIO EXT MIC I/F	
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Size Custom	Document Number 8540 API			Date:	Monday, August 12, 2019 Sheet 31 of 55

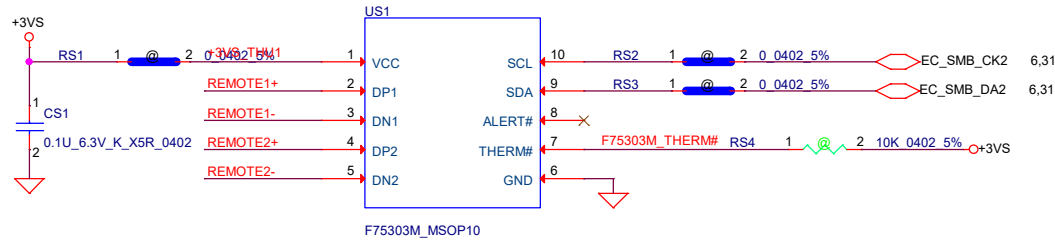




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				Custom	S540 API
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Thermal Sensor placed nearby SO-DIMM

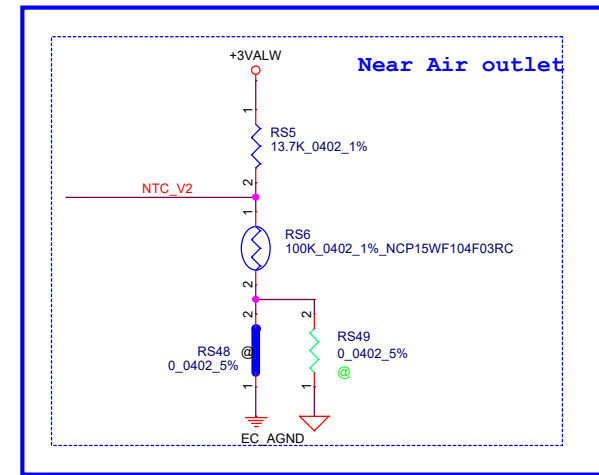


Address 1001_101xb

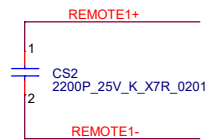
Internal pull up 1.2K to 1.5V

R for initial thermal shutdown temp

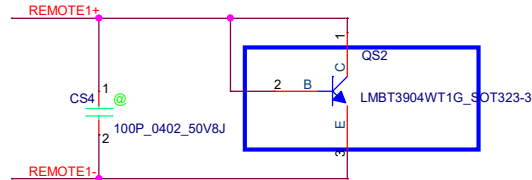
REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



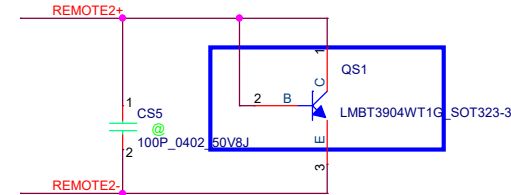
Close to U1



Close to Charger

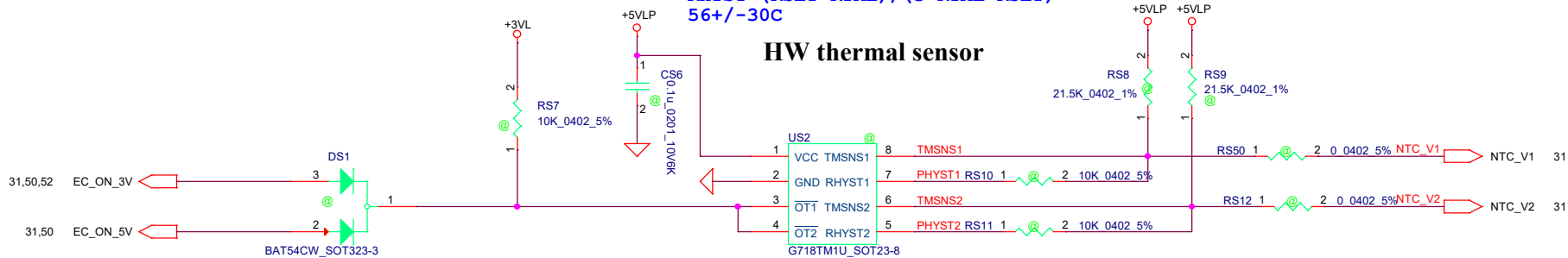


Close APU

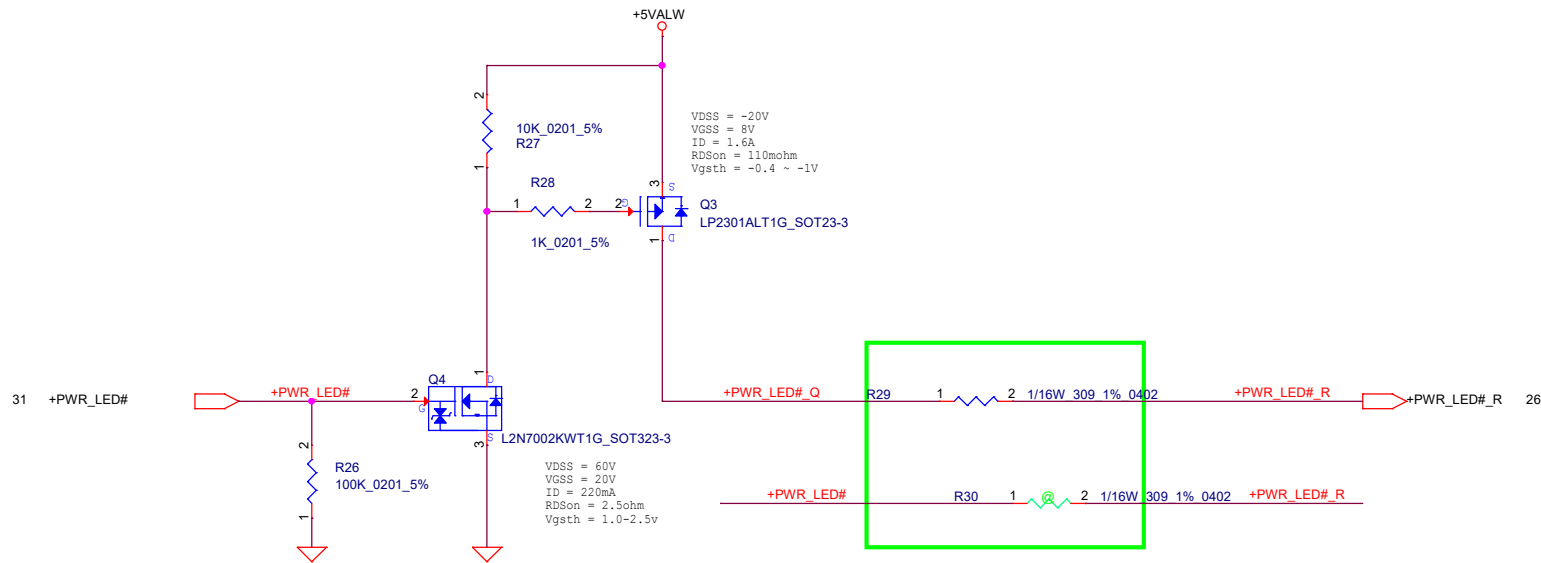
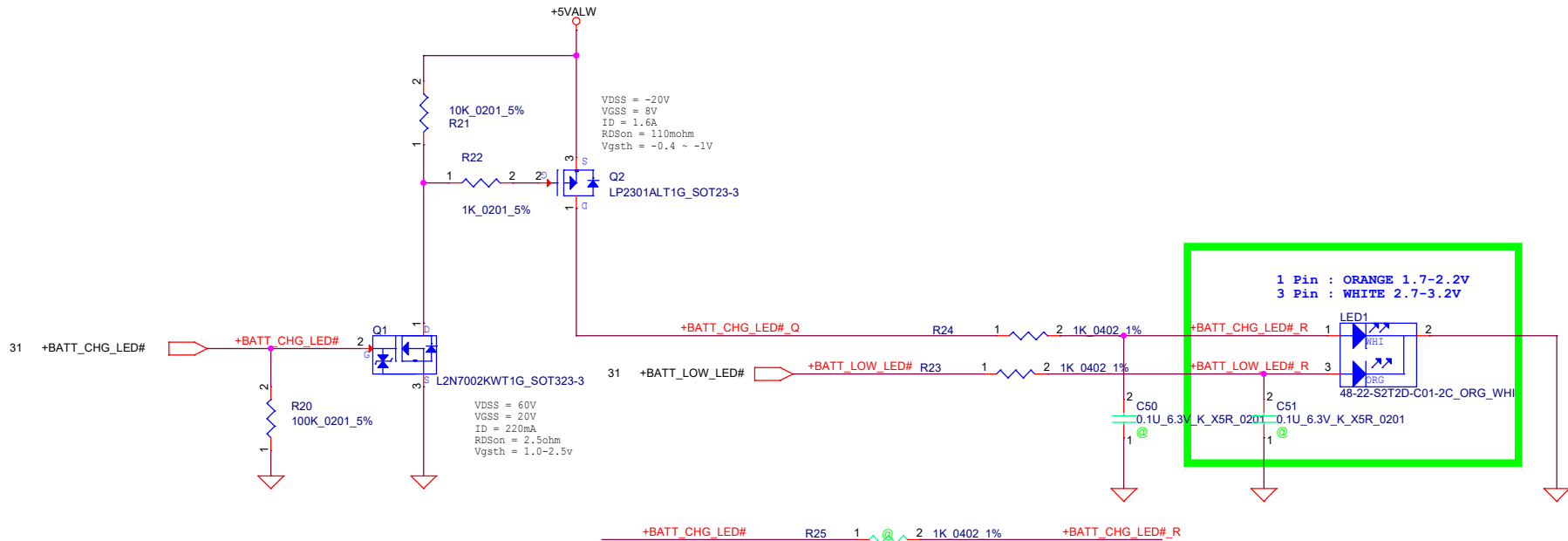



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST= (RSET*RTML) / (3*RTML-RSET)
56+/-30C

HW thermal sensor

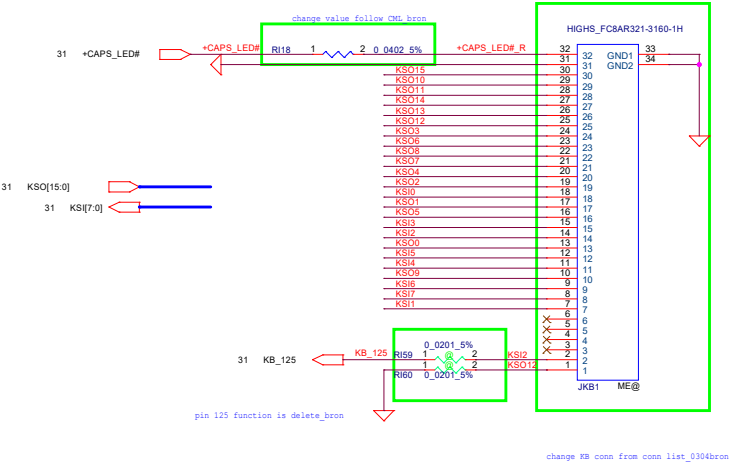
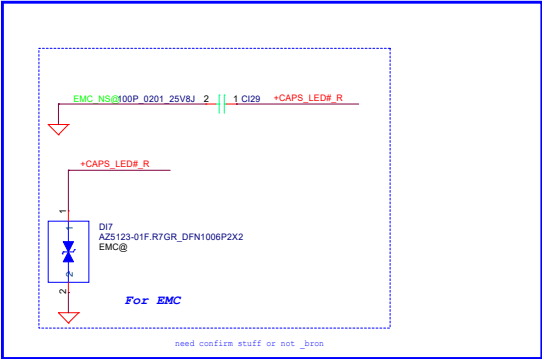


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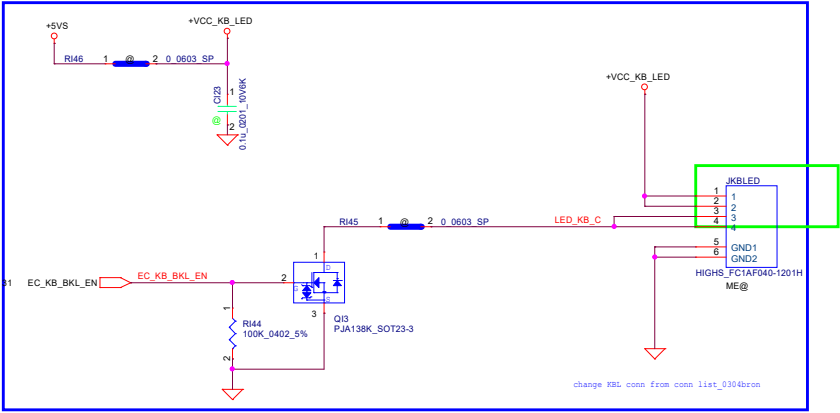


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KB Connector

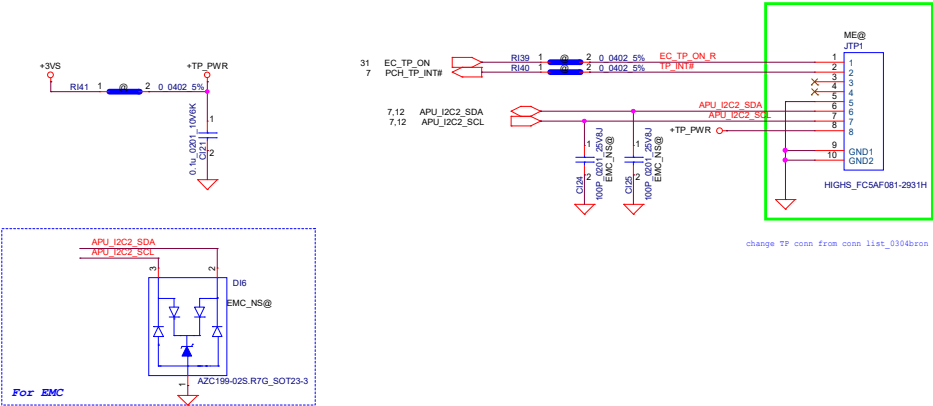


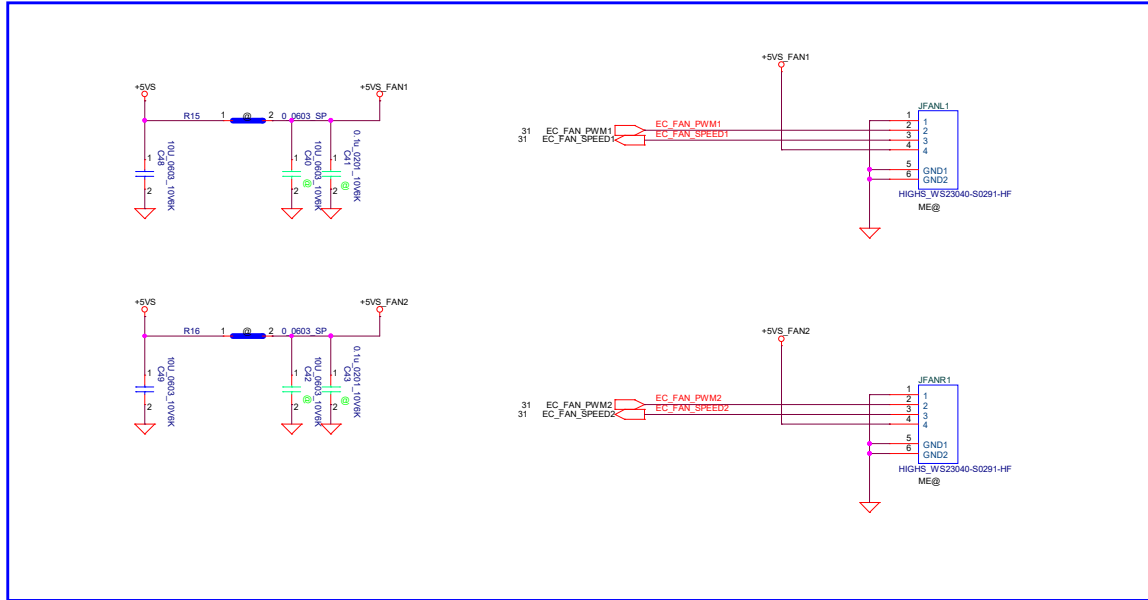
KB Backlight Connector



Security Classification	LC Future Center Secret Data			Title	KEYBOARD/TRACK POINT
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Normal TP





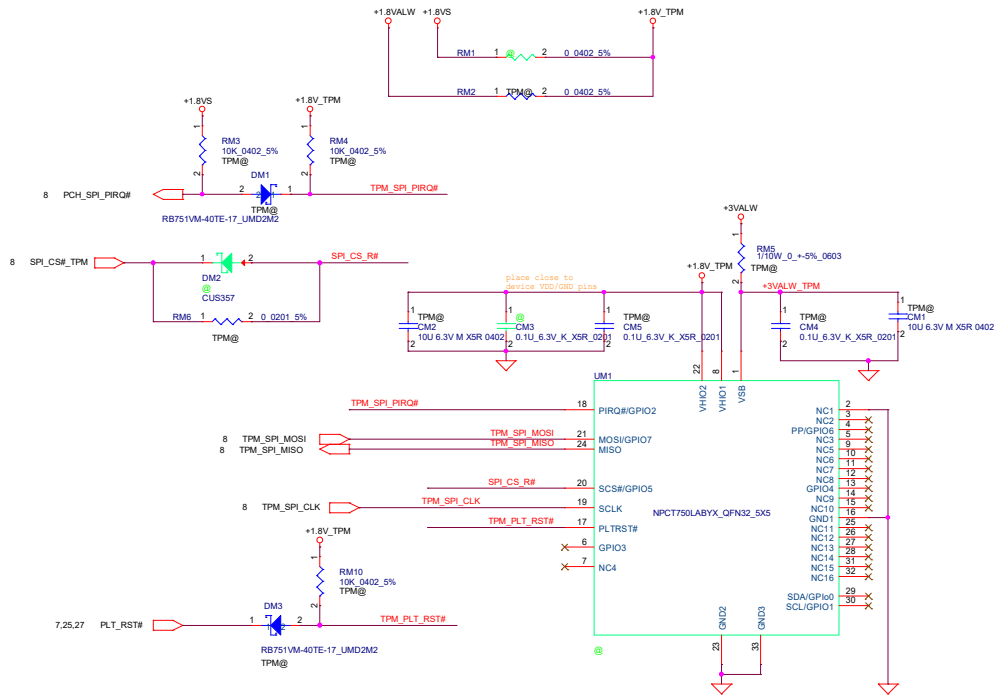
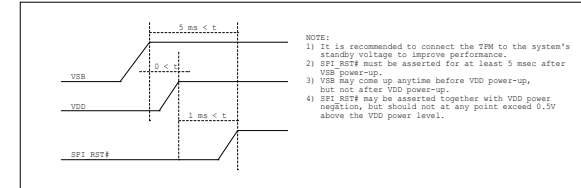


TABLE of TPM (U9801)		
Vendor	P/N	LCFC P/N
Nuvoton	NPCT750LABYX	SA00008KS10
ST Micro	ST33HTPH2E32AHC0	SA000089E20

Import Nuvoton on EVT

NOTE:
Check timing sequence in SDV phase.



TABLE

Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HTPH2E32AHC0
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	PP
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC

Load Switch
+5VALW To +5VS
+3VALW To +3VS

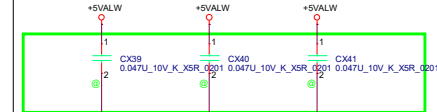
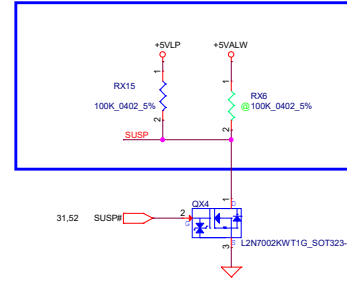
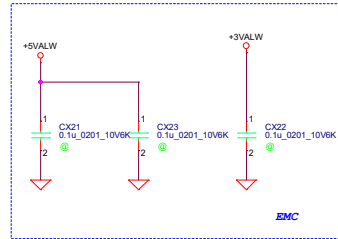
+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

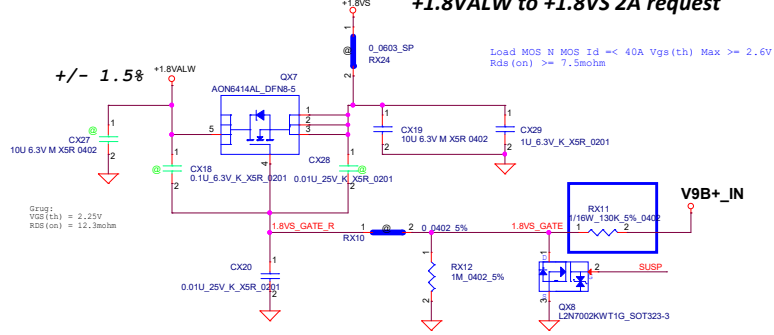
Need Short

Need Short

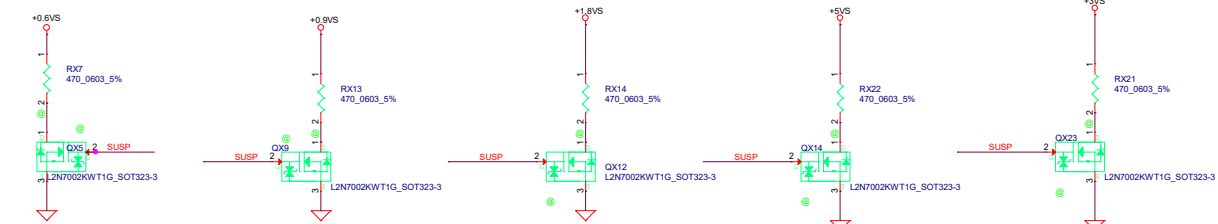
SA000067600 replace by SA00008F400 from common pool__bron



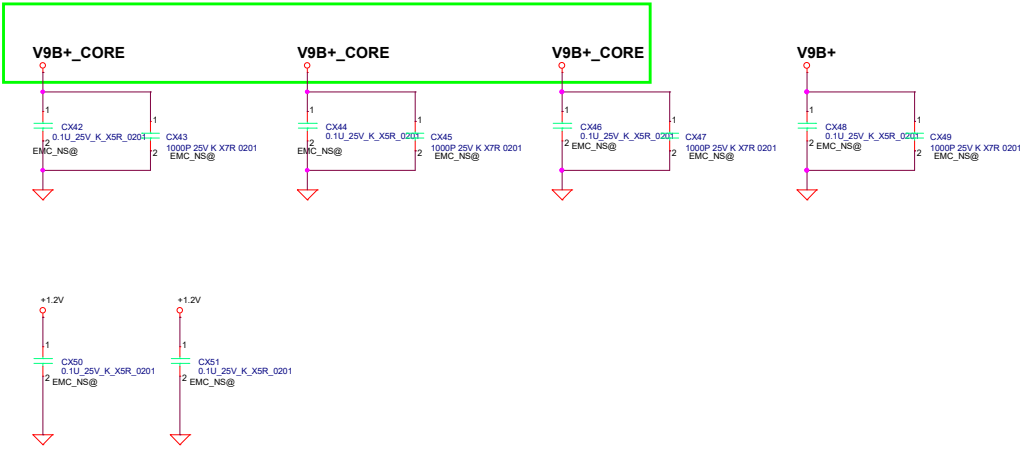
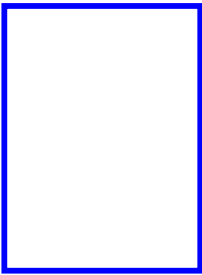
+1.8VALW to +1.8VS 2A request




For DisCharge




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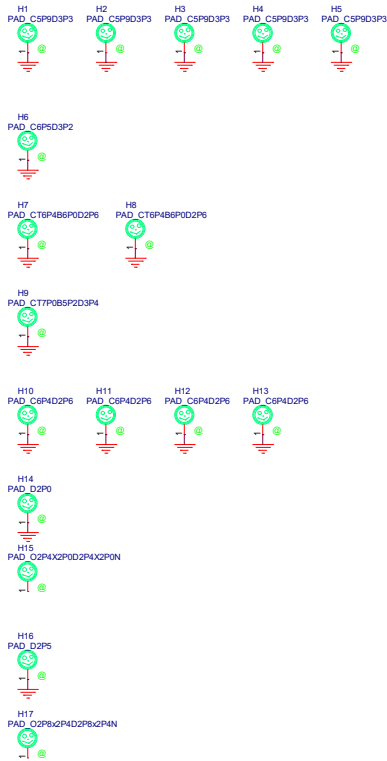




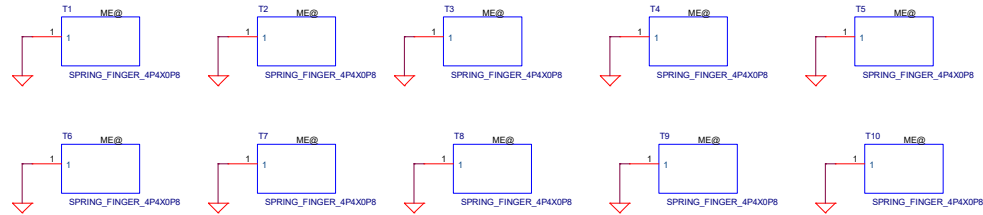
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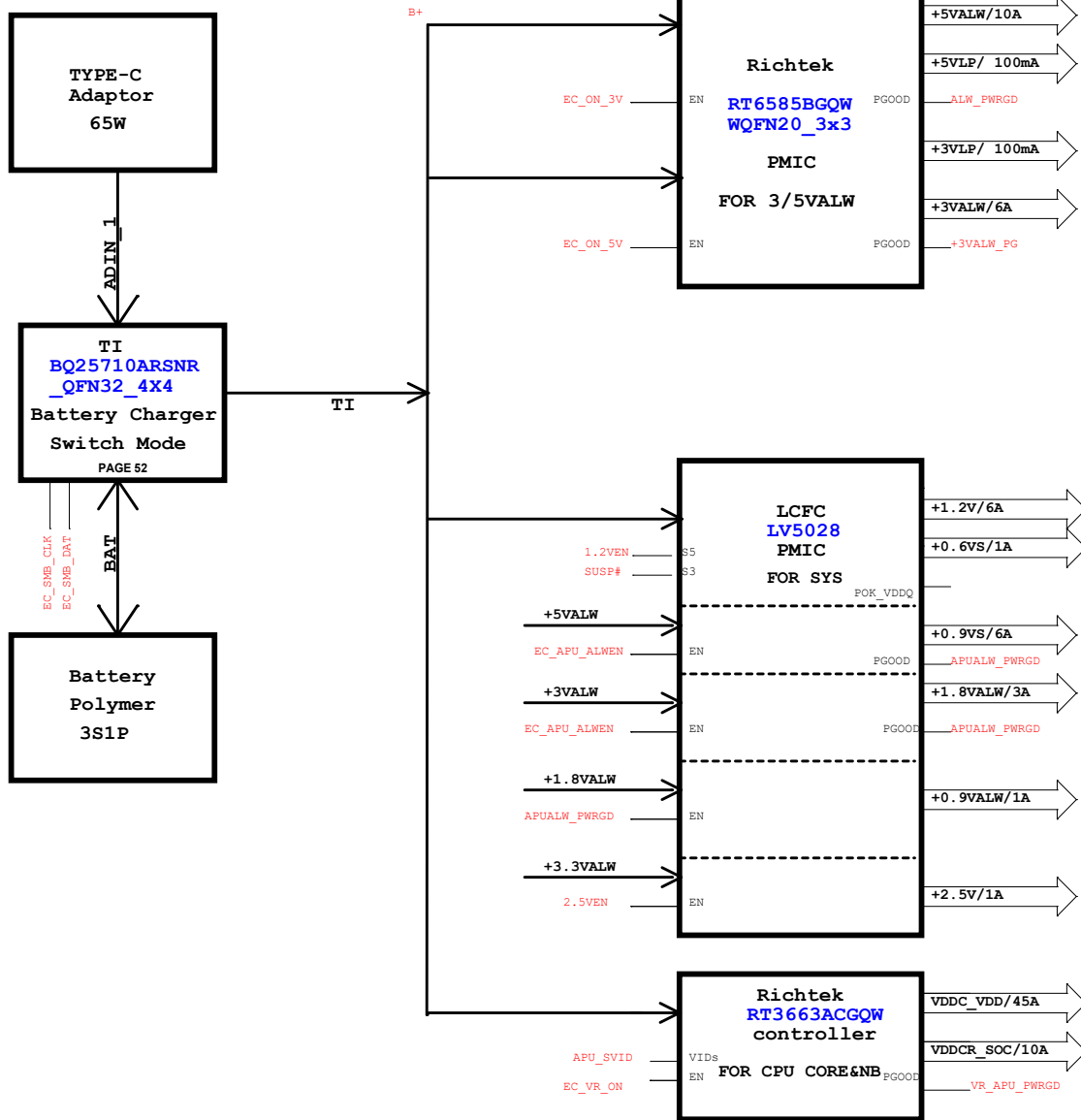
Shielding



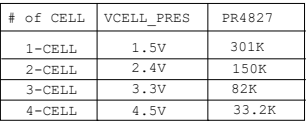
PCB Federal Mark PAD



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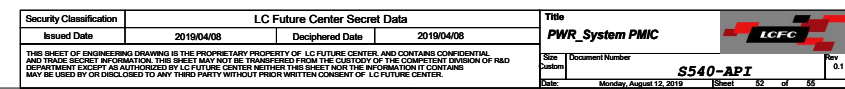
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C																								
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A																								

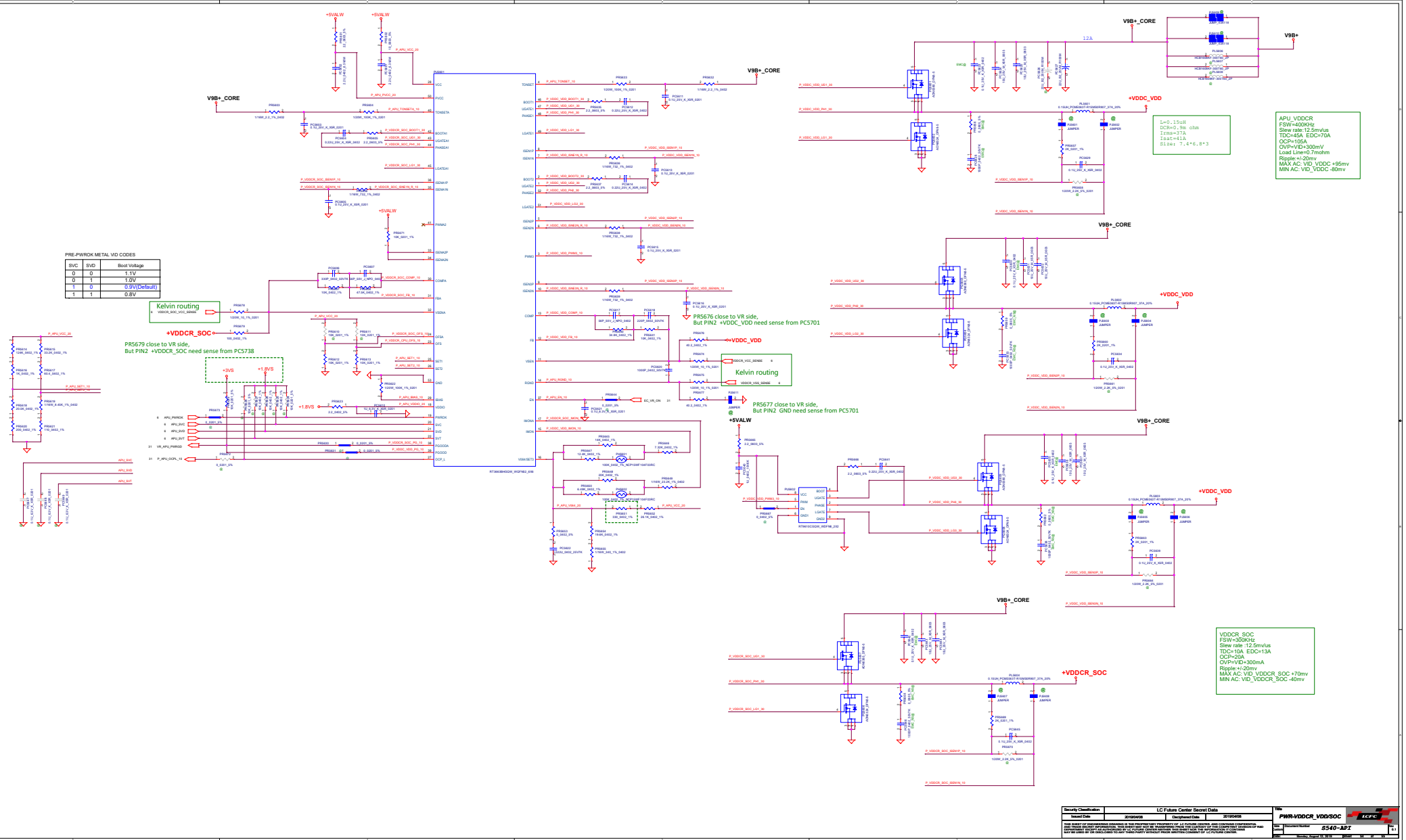


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D				D																				
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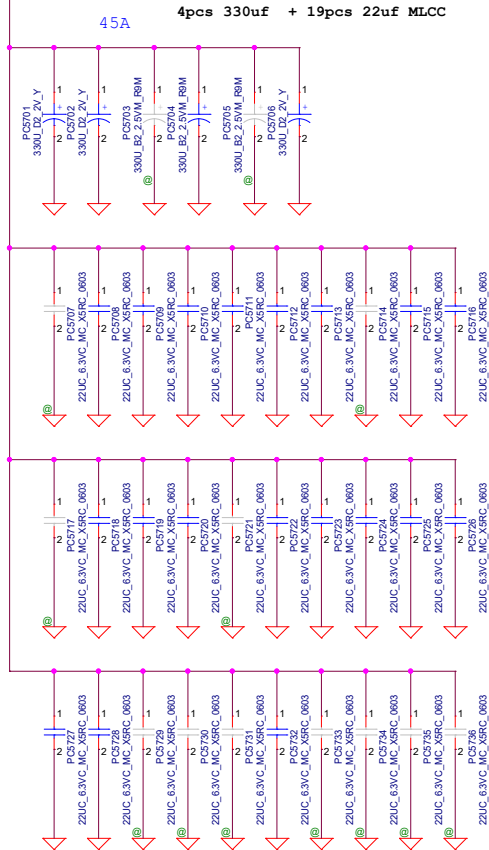


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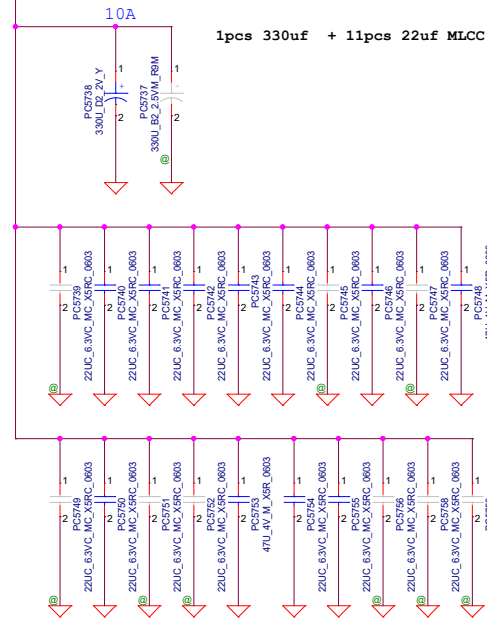




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